IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 5, May 2016

A Novel Modified Low Power Wallace Tree Multiplier Using Full and Half Adder: A Review

Swathi A.C[1], Yuvraj T [2], Praveen J [3], Raghavendra Rao A[4]

M.Tech Student, Dept. of ECE, Alva's Institute of Engg. & Technology, Mijar, Moodbidri, Karnataka, India[1]

Assistant Professor, Dept. of ECE, Alva's Institute of Engg. &Tech, Mijar, Moodbidri, Karnataka,India[2]

Sr. Associate Professor, Dept. of ECE, Alva's Institute of Engg. &Tech, Mijar, Moodbidri, Karnataka,India[3,4]

Abstract: Power utilization is a main sympathy toward all VLSI circuits architects. Arithmetic operations is done by multiplexer as far as shift and add operation. A Wallace tree multiplier is a rapid speed multiplier utilize full and half adder in the reduction stage. By outlining the reduced complexity Wallace multiplier to conventional Wallace multiplier the number MOS transistor is less. in the proposed method as far as area and power estimation of XOR-XNOR gates and MUX blocks discovered effective. The proposed phase of Wallace multiplier is performed with less area, power, and delay.

Keywords: Wallace tree multiplier, Multiplexer, Full adder, SAED90nm.

I. INTRODUCTION

In latest innovation fundamental component like area, delay and power utilization assumes a crucial part. The greater part of the advanced circuit needs number of handling units to outline fast, low power VLSI design. For a chip fashioner these are the essential configuration thought. The delay of any circuit correspondingly changes the required result and it is hard to get a precise result .Therefore here the research of this paper is to reduce the delay of multiplier. So that can easily reduce the delay of the whole circuit design. In this paper the main approach is Wallace tree multiplier. A Wallace tree multiplier is effective to product two whole numbers. It diminishes the quantity of partial product to be included into two last transitional results. Generation of partial item and including adding of multiplier is included in Wallace tree multiplier. In the second stage the era of this partial product gets into final to two rows. By using fast carry adder the adding of two rows gets done in the third phase. Numerous looks into has done to diminish the transition in the Wallace tree multiplier. Here the novel technique is utilized to diminished multiplier technique. Further change by adding one all the more half adder to the privilege most right segment and results area reduction. Area and also latency can be diminished by including booth encoding approach. In second stage approach the full adder and half adder gets changed with XOR-XNOR gates 3:2, 4:2 and 5:2 compressor results increment in speed of operation.

In the proposed technique the problastic gate level force estimation are utilized to assess the power in the every stage. To decrease the switching activity the generation of partial product item should reordered which is additionally a lead to reduction in power. The partial product items is gets distributed into four gathering. The dada gathering is gets connected to one gathering and Wallace multiplier is connected to another gathering to accomplish low power utilization.

In the reduction stage, to diminish the design constraint power 4:1 multiplexer are utilized with full adder. Absolutely there are six number of 2:1 multiplexer are gets actualized in the full adder. So that the engineering of this composed changed structure decrease the short circuit power and furthermore the transition activity will be less. Thus the force utilization is consequently done. The real burden is that gets range is essentially gets expanded.

A. RELATED WORK

In the Wallace Tree strategy, three single bit are gone to a one bit full adder which is called three input Wallace Tree circuit, and the yield signal (sum) is supplied to the next stage full adder of the same bit, and the carry output flag is gone to the next stage full adder of the same number of bit, and the carry output yield signal thereof is supplied to the next phase of the full adder located at one bit.

In the proposed Wallace tree multiplier for fast multiplication handle the process column compression technique. So that the total delay gets corresponding to logarithm of word length of multiplier operand. These column pressure Wallace multiplier is relatively speed than array multiplier. The delay in the array multiplier will differ straight though in the Wallace multiplier it fluctuates logarithmically.

Let us consider an example that N bits multiplication , N2 AND gates are required to generate the partial product terms and the number of reduction stages is given by S

$$s = \log 2^{N}$$

The hardware requirements is done in terms of full adder (FA) and the length of final adder (FAL) for diifernt size of Wallace multiplier is obtained.

Fig. 1 illustrates the reduction tree of 8 x 8 bits unsigned multiplier.

IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 5, May 2016

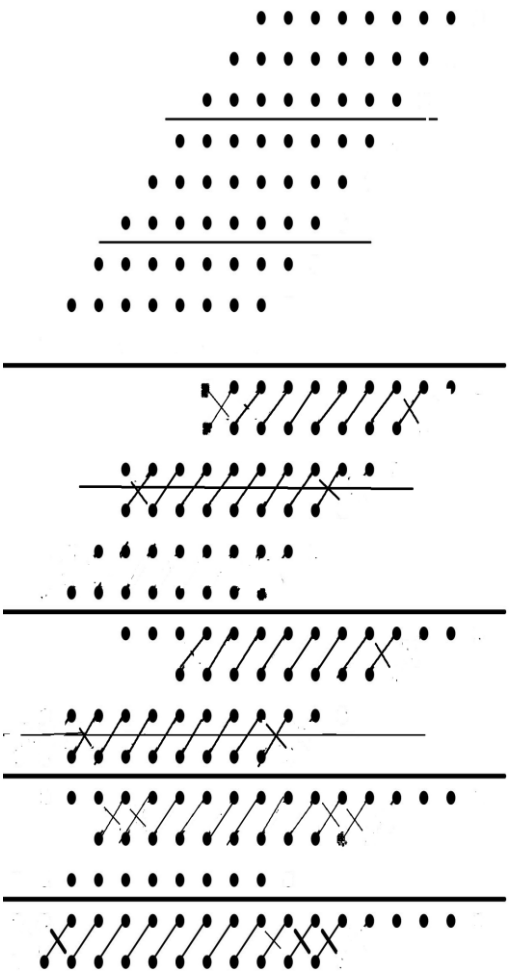

Fig. 1. 8-Bit Traditional Wallace Tree Multiplier

A 8bit Wallace tree multiplier is comprised of essentially two segments in particular half adder and full adder . so firstly half adder and full adder are outlined. For building 8 bit Wallace multiplier we require 8 half adder and 48 full adder so absolutely 56 adders are utilized. Hence , the half adder and full adder is instantiated for every calculation according to the requirement by passing the proper parameters. The last results is acquired from the sum and carry bits of the adder.

Each dot represents a single- bit partial product. Starting from the right most column, when three bits are come across, full adders and for two bits, half adders are used respectively. The sum and carry yields for every adder at one stage are again represented to as dots in the following stage and are utilized as inputs of adders as a part of that stage .Each column has a certain order of magnitude of the partial products. The sum output at one stage reflects a dot in.

$$FAL = (2N - 1) - S$$

in the same column at the next stage. The carry output at one stage reflects a dot in the column to its left i.e. one order of magnitude higher.

The final step of the Wallace tree-based multipliers is to add the remaining two rows using a fast adder. Some of the wires are widely used parallel-prefix adders used for high speed operations are Kogge-Stone , Sklansky , and Brent- Kung. These adders use the same tree topology but differ in terms of logic levels, fanout, and interconnect.

B. Conventional full adder:

In the reduction phase the conventional Wallace tree multiplier uses full adder . high power consumption is caused due to bottleneck of full adder. The conventional full adder is shown in the below figure (2).

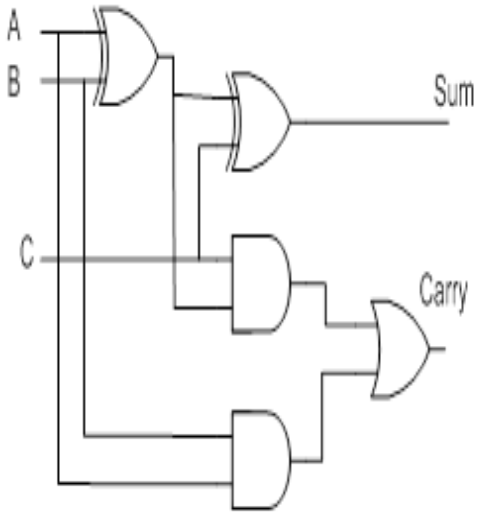

Fig.2 . Full adder

The above figure consists of two XOR gate and two AND gate and one OR gate. Here the main criteria is high power consumption and also includes increased in area. The critical path delay can be calculated as

$$Delay = 2 * XOR\ \Delta$$

C. Objective of the Project & Description:

The objective of the project is to In this paper The proposed and the existing multiplier designs are developed using Verilog HDL for 8 and 16 bits, respectively. The functionality of the 8-bit proposed Wallace tree multiplier is verified through simulations using cadence tool. The simulation waveform of Wallace tree multiplier using proposed full adder for 8-bits. All the multiplier designs are synthesized in Xilinx.

II. LITERATURE SURVEY

Writing review is an evaluative report of data found in writing identified with our chose area if study. The review should describe compress, assess and clear up the writing. It gives the hypothetical base of examination and helps us to decide the way of exploration.

The following section summarizes the literature survey carried out for the project.

Ron S. Waters Earl E. Swartzlander: The paper entitled as "A reduced complexity Wallace multiplier reduction," IEEE Transactions on Computers, vol. 59, no. 8, pp.1134-1137, 2010. In the year of 2010 presented on a Wallace reduction modification is ensures that the delay is the same as for the conventional Wallace reduction. Partial product

bits doesn't reduce by half adder. Hence by reducing the count of half adder will reduce the complexity of design. In this paper instead of using half adder slightly increase the count of full adder[2].

Shahzad Asif and Yinan Kong: This paper is based on area of Wallace multiplier and published I the year 2014 "Low Area Wallace Multiplier,"**.** The proposed architecture Wallace multiplier reduces the count of half adder called it as RCW multiplier and it is excepted same as TW multiplier. The synthesis is done based on Synopsys design complier in 90nm technology. The future work is to design using Synopsys IC complier to analyze post layout results for area and delay[3].

S.Karthick, S.Karthika, S.Valarmathy: In this paper the enhancement is done both on booth multiplier that is parallel multiplier and Wallace tree multiplier. 14 transistor adder cell is compared with 3-2, 4-2, 5-2, compressor design with different logic. Hence the result is low transition , low power consumption and high speed.

International Journal of Advanced Research in Electrical, Electronics and instrumentation Engineering, You, Issue 6, Dec. 2012[5].

C. S. Wallace: The paper is entitles as "A suggestion for a fast multiplier," IEEE Transaction on Electronic Computers, Vol. EC-13, pp.14-17.This paper describes the high speed design multiplication-division method unit. This paper research is done on multiplier unit . it is an efficient to use and it is used only for some arithmetic operation of 30nsec delay[1].

Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung:
This paper presents a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). The simulation is done using HSPICE on new MBA-12T allows lower transition count and results lower internal capacitance. The major disadvantage is area is comparatively more than conventional method since of adding new adder in the proposed method[9].

M Jagadeshwar Rao, Sanjay Dubey: In this paper the proposed method is based on booth recorder and it improves architecture of Wallace tree multiplier the aim of this paper is to reduce the latecncy and area of the designed method. The process is carried over by using algorithm Booth algorithm and compressor adders. The propose method is 67 per faster than conventional method. IEEE transactions on circuits and systems, vol. 51, no. 7, July 2004, pp.345-348[4].

S. T. Oskuii, P. G. Kjeldsberg: "Power optimized partial product reduction interconnect ordering in parallel multipliers," NORCHIP, Aalborg, 19-20 Nov. 2007, pp.1-6.The paper presentation is based on generation of power efficient parallel multiplier hence here the partial product bit is connected to minimise activity. Internal partial product will vary significantly for different partial product[6].

M. V. P. Kumar, S. Sivanantham, S. Balamurugan, P. S. Mallick presented on "Low power reconfigurable multiplier with reordering of partial products," **.**Generally in any processor multipliers results increase in power, area and time. And also multiplier is main key element for any computation so here the main is to reduce the area and power consumption. Twin precision multiplier is an efficient multiplier that overcomes the drawback of conventional full precision multiplier. Reordering partial products is applied on both high performance multiplier and dada column reduction**.**

International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), Thuckafay, 21-22 July 2011, pp.532-536[7].

P. Anitha, P. Ramanathan, presented paper on "A new hybrid multiplier using Dadda and Wallace method," in International Conference on Electronics and Communication Systems (ICECS), Coimbatore, India, 13-14 Feb. 2014, pp.1-4.In this paper presentation the enhancement of 8*8 hybrid tree multiplier is done by combining both Wallace tree multiplier and also by dadda methods. The design and simulation is done by DSCH2 and MICROWIND tool[8].

S. Murugeswari, S. K. Mohideen, "Design of area efficient and low power multipliers using multiplexer based full adder," in 2nd International Conference on Current Trends in Engineering and technology (ICCTET), Enathi, India, July 2014, pp.388-392. The Wallace tree multiplier and dadda multiplier has developed in the year 1964 and 1965.

The author present on the area of multiplier with fewer components and less interconnect wires. The reduction scheme is useful for pipelined multipliers, because it minizies the number of latches required in the reduction of partial product. Area estimate indicates that pipelined reduced area multipliers require 3 to 8 %less area than existing Wallace tree multipliers[10].

III. APPLICATION

Shahzad Asif and Yinan Kong presented paper on low area Wallace tree multiplier **.** The power of the proposed multiplier can be explored to implement high performance multiplier in VLSI applications. Wallace tree multiplier using booth algorithm ia very good technique for high speed applications, its implement with different logics in VLSI design[3].

C. S. Wallace works on fast multiplier. The fast multiplier are implemenyted in high speed signal processing that includes DSP based application. Wallace tree multiplier are used in DWT and DCT transformer used for image and wide signal processing.The fast multiplier are used in FIR and IIR filters for high speed , low power filtering application. And also used in multirate signal processing applications such as digital down converters and up converters[1].

P. Anitha, P. Ramanathan designed 8*8 hybrid multiplier. Multiplier is major source of power dissipation in application like digital signal processing , microprocessor and application specific inyegrated circuit. Performance of high speed multiplication is a primary requirement of high performance computing systems[8].

IV. CONCLUSION

In this paper, a multiplexers using full adder of Wallace tree multiplier and xor gate gets modified so that the area can be reduced. In reduction phase by implementing a modified full adder of Wallace tree an average power, area and delay is reduced, compared to existing methods respectively is achieved. The synthesis result confirms that the proposed Wallace tree multiplier is suitable for low power and small area applications. The designs are synthesized in Synopsys Design Compiler using SAED90nm CMOS technology.

REFERNCES

[1] Wallace, "A suggestion for a fast multiplier," IEEE Transaction on Electronic Computers, Vol. EC-13, pp.14-17.
[2] R. S. Waters, E. E. Swartzlander, "A reduced complexity Wallace multiplier reduction," IEEE Transactions on Computers, vol. 59, no. 8, pp.1134-1137, 2010.
[3] Shahzad Asif and Yinan Kong, "Low Area Wallace Multiplier," VLSI Design, vol. 2014.
[4] M. J. Rao, S. Dubey, "A high speed and area efficient Booth recoded Wallace tree multiplier for Fast Arithmetic Circuits," in Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Hyderabad, India, 5-7 Dec. 2012, pp.220-223.
[5] Karthick, S. Karthika and S. Valannathy, "Design and Analysis of Low Power Compressors," International Journal of Advanced Research in Electrical, Electronics and instrumentation Engineering, YoU, Issue 6, Dec. 2012.
[6] S. T. Oskuii, P. G. Kjeldsberg, "Power optimized partial product reduction interconnect ordering in parallel multipliers," NORCHIP, Aalborg, 19-20 Nov. 2007, pp.1-6.
[7] M. V. P. Kumar, S. Sivanantham, S. Balamurugan, P. S. Mallick, "Low power reconfigurable multiplier with reordering of partial products," in International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), Thuckafay, 21-22 July 2011, pp.532-536.
[8] P. Anitha, P. Ramanathan, "A new hybrid multiplier using Dadda and Wallace method," in International Conference on Electronics and Communication Systems (ICECS), Coimbatore, India, 13-14 Feb. 2014, pp.1-4.
[9] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder," IEEE transactions on circuits and systems, vol. 51, no. 7, July 2004, pp. 345-348.
[10] S. Murugeswari, S. K. Mohideen, "Design of area efficient and low power multipliers using multiplexer based full adder," in 2nd International Conference on Current Trends in Engineering and technology (ICCTET), Enathi, India, July 2014, pp.388-392.